[0069] A structure of the device edge termination portion is not particularly described, however, any edge termination structure such as a RESURF (Reduced SURface Field) structure and a guard ring structure can be used for implement.

[0070] Moreover, even if the bottom of the p-type pillar layer **4** is in contact with the drain layer **2**, the similar effect is achieved. Even if a layer containing a lower impurity concentration than the n-type pillar layer **3** is inserted between the super junction structure and the drain layer **2**, implement is possible similarly.

[0071] The MOSFET based on silicon (Si) as a semiconductor has been described, however, the semiconductor can be illustratively based on a compound semiconductor such as silicon carbide (SiC) and gallium nitride (GaN), and a wide gap semiconductor such as diamond.

1. A semiconductor device comprising:
- a first semiconductor layer of a first conductivity type;
- a second semiconductor layer of a first conductivity type provided on a major surface of the first semiconductor layer;
- a third semiconductor layer of a second conductivity type provided above the major surface of the first semiconductor layer adjacent to the second semiconductor layer, and forming a periodical arrangement structure in conjunction with the second semiconductor layer in a lateral direction generally parallel to the major surface of the first semiconductor layer;
- a fourth semiconductor layer of a second conductivity type provided on the third semiconductor layer;
- a fifth semiconductor layer of a first conductivity type selectively provided on a surface of the fourth semiconductor layer;
- a first main electrode electrically connected to the first semiconductor layer;
- a gate insulating film provided on a portion being in contact with the fourth semiconductor layer, a portion being in contact with the fifth semiconductor layer and a portion being in contact with the second semiconductor layer;
- a control electrode provided opposed to the fourth semiconductor layer, the fifth semiconductor layer and the second semiconductor layer via the gate insulating film; and
- a second main electrode electrically connected to the fourth semiconductor layer, the fifth semiconductor layer and the second semiconductor layer,
- the second main electrode being in contact with a surface of the second semiconductor layer located between the control electrodes to form a Schottky junction.

2. The device according to claim **1**, wherein the control electrode is provided above a junction interface between the second semiconductor layer and the third semiconductor layer via the gate insulating film.

3. The device according to claim **1**, wherein the gate insulating film and the control electrode are provided in a trench formed in contact with the fourth semiconductor layer, the fifth semiconductor layer and the second semiconductor layer.

4. The device according to claim **3**, wherein the second main electrode is in contact with the surface of the second semiconductor layer with a width narrower than a depth of the trench.

5. The device according to claim **3**, wherein a sixth semiconductor layer of a second conductivity type is selectively provided on the surface of the second semiconductor layer.

6. The device according to claim **5**, wherein the sixth semiconductor layer is provided at a center of the surface of the second semiconductor layer and not in contact with the gate insulating film.

7. The device according to claim **1**, wherein
- the gate insulating film and the control electrode are provided in a trench formed in contact with the fourth semiconductor layer, the fifth semiconductor layer and the second semiconductor layer,
- a sixth semiconductor layer of a second conductivity is selectively provided on the surface of the second semiconductor layer, and
- the trench and the sixth semiconductor layer are formed in a striped configuration orthogonal to each other.

8. The device according to claim **1**, wherein
- the gate insulating film and the control electrode are provided in a trench formed in contact with the fourth semiconductor layer, the fifth semiconductor layer and the second semiconductor layer, and
- a bottom depth of the fourth semiconductor layer is larger than a bottom depth of the trench.

9. The device according to claim **8**, wherein a sixth semiconductor layer of a second conductivity type is selectively provided on the surface of the second semiconductor layer.

10. The device according to claim **1**, wherein
- the gate insulating film and the control electrode are provided in a first trench formed in contact with the fourth semiconductor layer, the fifth semiconductor layer and the second semiconductor layer, and
- a second trench is provided on a superficial portion of the second semiconductor layer.

11. The device according to claim **10**, wherein the same material as the gate insulating film and the control electrode is embedded inside the second trench.

12. The device according to claim. **10**, wherein
- a sixth semiconductor layer of a second conductivity type is provided on a bottom of the second trench, and
- the second main electrode is embedded inside the second trench.

13. The device according to claim **1**, wherein the gate insulating film and the control electrode include a planar gate structure.

14. The device according to claim **13**, wherein a sixth semiconductor layer of a second conductivity type is selectively provided on the surface of the second semiconductor layer.

15. The device according to claim **1**, wherein a width of the third semiconductor layer is narrower than a width of the second semiconductor layer.

16. The device according to claim **15**, wherein
- a lateral period of the third semiconductor layer is **1/2** times of a lateral period of the fourth semiconductor layer, and
- the third semiconductor layer not in contact with the fourth semiconductor layer is in contact with the second main electrode.

17. The device according to claim **16**, wherein a seventh semiconductor layer of a second conductivity type is provided on a surface of the third semiconductor layer in contact with the second main electrode.

18. The device according to claim **17**, wherein the seventh semiconductor layer has a higher second conductivity type impurity concentration than the third semiconductor layer.

19. The device according to claim **1**, wherein a transistor including the fourth semiconductor layer and the fifth semi-